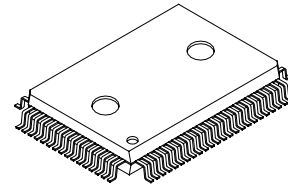


CMOS 4-bit Single Chip Microcomputer

Description

CXP5076/5078 is a CMOS 4-bit microcomputer which consists of 4-bit CPU, ROM, RAM, I/O port, 8-bit timer, 8-bit timer/counter, 18-bit time base timer, 8-bit serial I/O, vector interruption, power on reset function, liquid crystal displayer (LCD) controller/driver, D/A conversion 14-bit PWM output port, a remote control reception circuit with noise eliminating circuit, 3-bit A/D converters, a 32kHz timer/event counter and a power supply voltage detection reset function. They are integrated into a single chip with the standby function, etc. which are to be operated at a low power consumption.

80 pin QFP (Plastic)



Features

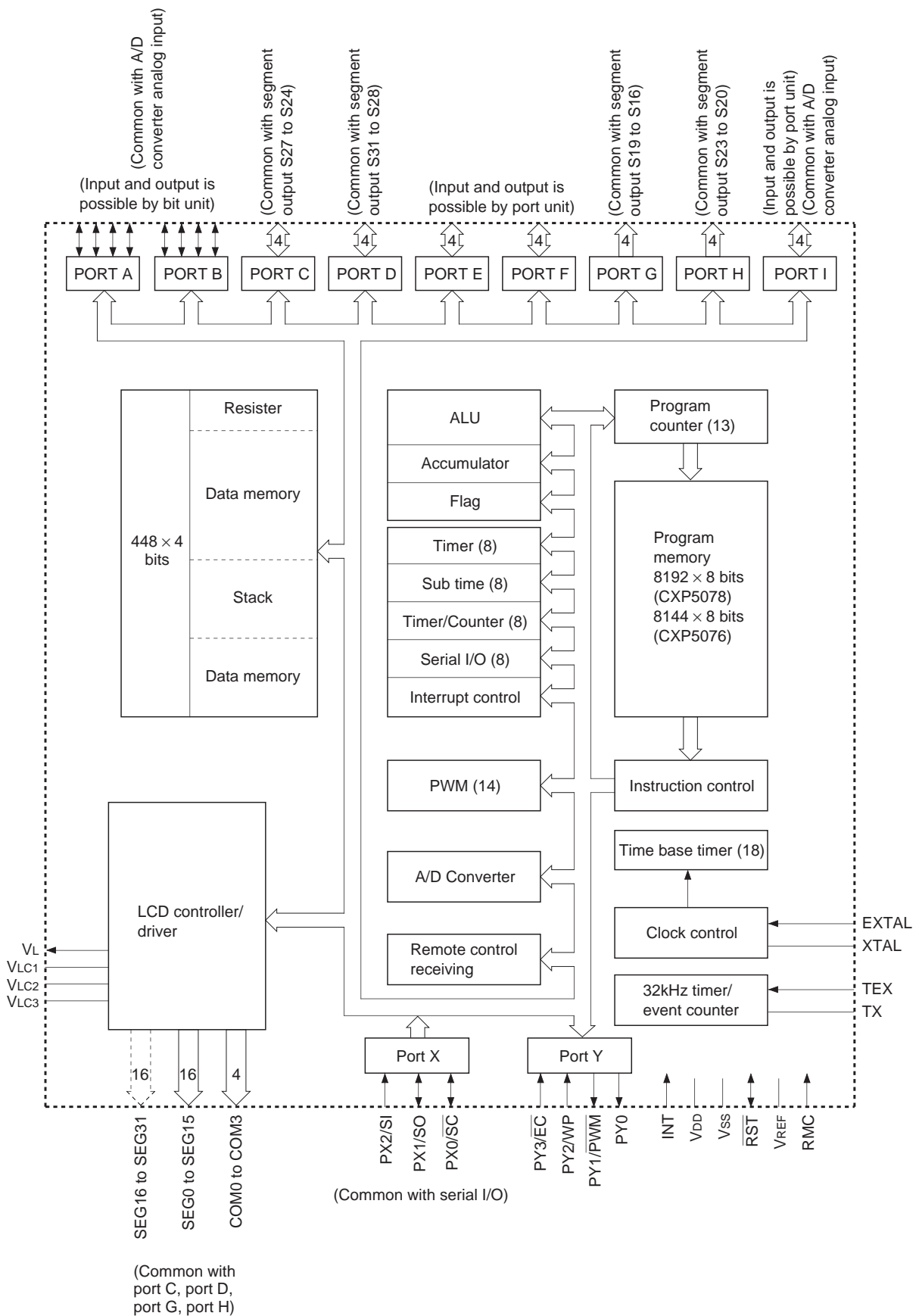
- Instruction cycle 1.9 μ s/4.19MHz
122 μ s/32kHz
(Possible to select with the program)
- ROM capacity 8192 \times 8 bits (CXP5078)
6144 \times 8 bits (CXP5076)
- RAM capacity 448 \times 4 bits (Including stack, display area)
- 43 general purpose I/O ports
- 8 high current output ports
- LCD controller/driver (Possible to direct drive)
 - Possible to select with the program the segment output of 16 to 32
 - Possible to select with the program the duty of static, 1/2, 1/3 and 1/4
 - Possible to select with the program the bias of 1/2, 1/3
- 14-bit PWM output for D/A conversion
- Remote control reception circuit
- 3-bit A/D converter (8 channels per circuit)
- 32kHz timer/event counter
- Power supply voltage detection reset function
- Low voltage operation (2.5V) when operating in 122 μ s/32kHz
- Rich wake-up function
- 8-bit/4-bit variable serial I/O
- Arithmetic and logical operations possible between the entire ROM area, I/O area and the accumulator by means of the memory mapped I/O
- 8-bit timer, 8-bit timer/event counter and 18-bit time base timer, independently controlled
- 2 kinds of power down modes of sleep and stop
- Power on reset circuit (mask option)
- Provided with 80 pin plastic QFP
- Provided with 80 pin piggyback QFP (CXP5070)

Structure

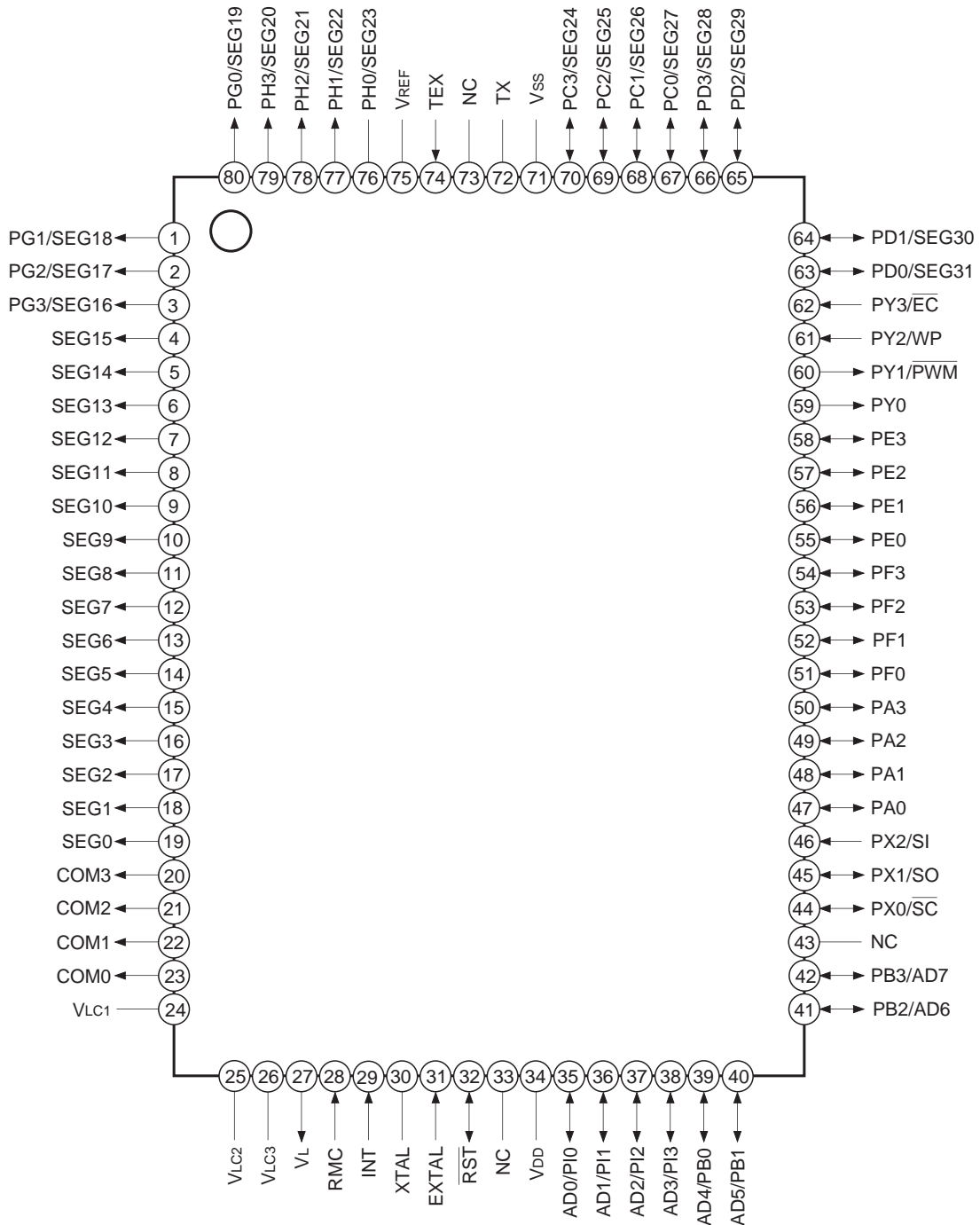
Silicon gate CMOS IC

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Block Diagram

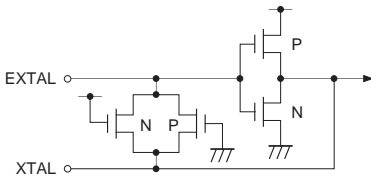
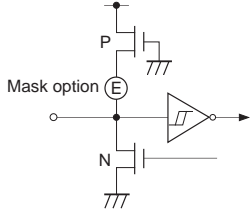
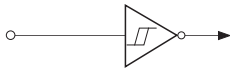
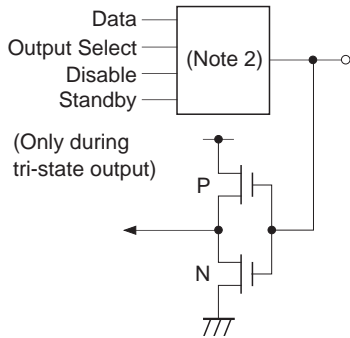


Pin Configuration (Top View)

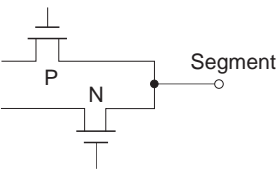
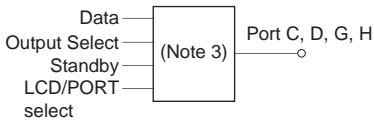
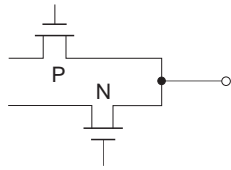
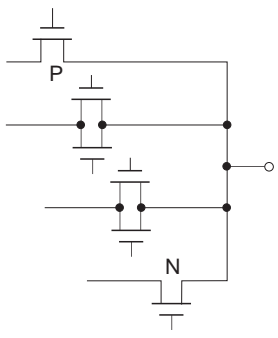
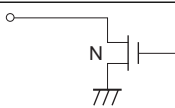


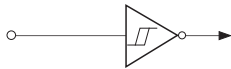
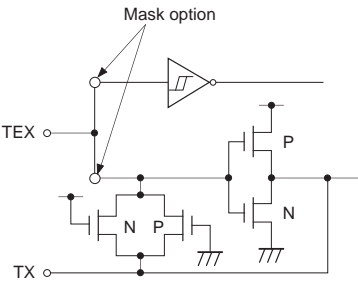
Note) Do not make any connections to NC pins.

Pin Description

Symbol	Name	I/O	Equivalent Circuit	Description
V _{DD}	Supply voltage	—		Positive voltage supply pin
V _{SS}	Grounding voltage	—		GND pin
EXTAL	Clock input	I		Clock oscillation circuit input pin. Connect the crystal oscillator or ceramic resonator between the EXTAL and XTAL. When using as the external clock input, connect the clock oscillation source to the EXTAL pin and open the XTAL pin.
XTAL	Clock output	O		Clock oscillation circuit output pin
$\overline{\text{RST}}$	Reset	I/O	 <p>Output pull-up resistor (P-ch Tr) N-ch Tr output Schmitt inverter input</p>	Serves as the incorporated power-on reset circuit output pin. When inputting a reset signal from the outside, provide 2 instruction cycles or longer of an "L" level (0V).
INT	External interrupt	I		Serves the interrupt input pin. Permits the selection with a program of the edge and the level modes.
RMC	Remote control input	I	Schmitt inverter input	Remote control receiver input pin
PX2/SI	Port X2 Serial input	I		Doubles as a serial interface (8 bits) input pin and as bit "2" (input) of port X.
PX1/SO	Port X1 Serial output	I/O	 <p>See Note 2) for the output circuit format. Inverter input</p>	Doubles as a serial interface (8 bits) output pin and as bit "1" (input) of port X. (SO output possible to inhibit with the program.)

Symbol	Name	I/O	Equivalent Circuit	Description
PX0/ \overline{SC}	Port X0 Serial clock	I/O	<p>(Only during tri-state output)</p> <p>See Note 2) for the output circuit format. Schmitt inverter input</p>	Doubles as shift clock input/output pin for the serial interface and as bit "0" (input) of port X.
PY3/ \overline{EC}	Port Y3 Event count input	I	<p>Schmitt inverter input</p>	Doubles as event counter (8 bits) input pin and as bit "3" (input) of port Y.
PY2/WP	Port Y2 Wake-up input	I		Doubles as wake-up input pin to release the standby state and as bit "2" (input) of port Y.
PY1/ \overline{PWM}	Port Y1 PWM generator output	O	<p>See Note 1) for the output circuit format.</p>	Doubles as PWM generator (14 bits) output pin and as bit "1" (output) of port Y.
PY0	Port Y0	O		Output pin for bit "0" of port Y.
PA0 to PA3	Port A	I/O	<p>(Only during tri-state output)</p> <p>See Note 2) for the output circuit format. Inverter input</p>	This 4-bit input/output port permits its each individual bit to be programmed to serve either as input or output. For the output format, a tri-state and pull-up resistor possible to be programmed, and it is also used as the standby resetting pin.
PB0/AD4 to PB3/AD7	Port B Analog voltage input	I/O		This 4-bit input/output port has the functions that are equivalent to those of port A. It is also used for A/D converter input.
PE0 to PE3	Port E	I/O		This 4-bit input/output port permits its each individual port to be programmed to serve either as input or output. For the output format, a tri-state and pull-up resistor possible to be programmed.
PF0 to PF3	Port F	I/O		This 4-bit input/output port has the functions that are equivalent to those of port E.
PI0/AD0 to PI3/AD3	Port I Analog voltage input	I/O		This 4-bit input/output port has the functions that are equivalent to those of port E. It is also used for A/D converter input.

Symbol	Name	I/O	Equivalent Circuit	Description
PD3/ SEG31 to PD0/ SEG28	Port D Segment output	O		Doubles as a 4-bit output port (For the output format, the inverter and pull-up resistor possible to be programmed.) and as the segment signal output pin for LCD.
PC3/ SEG27 to PC0/ SEG24	Port C Segment output	O	The transfer gate input signal is controlled based on 1/2, 1/3 bias method in advance.	Doubles as a 4-bit output port (The output format is equivalent to port D.) and as the segment signal output pin for LCD.
PH3/ SEG23 to PH0/ SEG20	Port H Segment output	O	 See Note 3) for the output circuit format.	Doubles as a 4-bit output port (The output format is equivalent to port D.) and as the segment signal output pin for LCD. (Possible to designate in bit units.)
PG3/ SEG19 to PG0/ SEG16	Port G Segment output	O	The transfer gate input signal is controlled based on 1/2, 1/3 bias methods in advance.	Doubles as a 4-bit output port (The output format is equivalent to port D.) and as the segment signal output pin for LCD.
SEG0 to SEG15	Segment output	O		Segment signal output pin for LCD
COM0 to COM3	Common output	O	 Transfer gate output	Common signal output pin for LCD
VLc1 to VLc3	Power supply for LCD	—		Bias power supply pin for LCD
VL	Cut-off output	O		Control pin which cuts off the current input to the bias resistor for the external LCD during standby.

Symbol	Name	I/O	Equivalent Circuit	Description
WP	Wake-up input	I	 <p>Schmitt inverter input</p>	It is the input pin to release the standby mode, and release by "1".
TEX	32kHz T/C clock input	I		Input pin for 32kHz timer clock generation circuit. Connect the 32.768kHz crystal oscillator between TEX and TX. When using as the event clock input, connect the clock oscillation source to the TEX pin, open the TX pin.
TX	32kHz T/C clock output	O		Output of clock generation circuit
V _{REF}	Reference voltage input	I		Reference voltage input for power supply voltage resetting circuit. Connect the zener diode normally.

For all output ports, the output states of ports during standby possible to be programmed to the state holding before standby or the change to the high impedance.

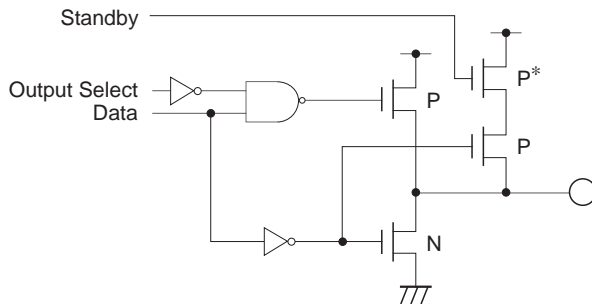
When the pull-up resistor output is selected, it becomes a pulled-up state even it is input port.

During standby, it is impossible to change to the high impedance of PY0 and PY1 in the inverter output state. To change to the high impedance, select the pull-up resistor output, and then set to the high level output ("1" state).

Note 1) Possible to select out of the following two ways for the output circuit format.

(port units: programmable)

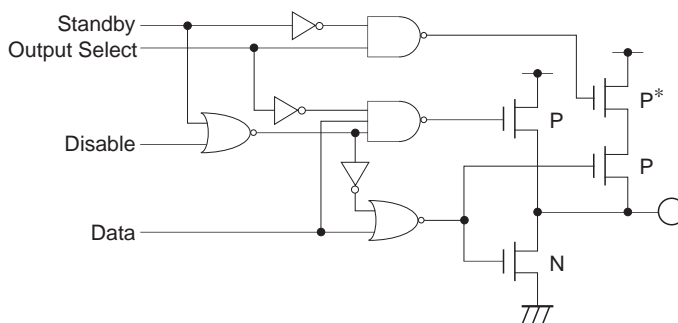
- (a) Inverter output
- (b) Pull-up resistor output



Note 2) Possible to select out of the following two ways for the output circuit format.

(port units: programmable)

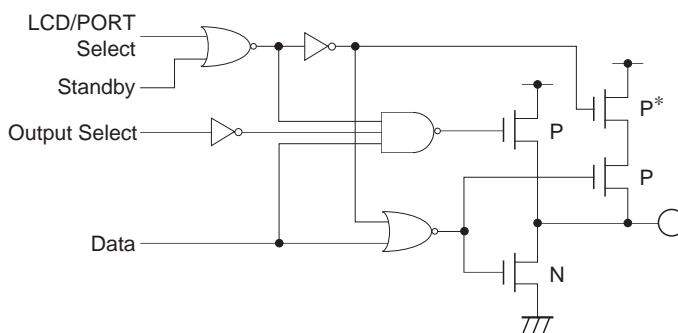
- (a) Tri-state output
- (b) Pull-up resistor output



Note 3) Possible to select out of the following two ways for the output circuit format.

(port units: programmable)

- (a) Inverter output
- (b) Pull-up resistor output



* As the output pull-up resistor is CMOS pull-up output of about 10kΩ, the pull-up resistor becomes OFF state during "L" output.

Absolute Maximum Ratings

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V _{DD}	-0.3 to +7.0	V	
LCD bias voltage	V _{CL1} , V _{CL2} , V _{CL3}	-0.3 to +7.0* ¹	V	
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
High level output current	I _{OH}	-5	mA	General purpose port* ² : per pin
High level total output current	∑I _{OH}	-50	mA	Entire pins total
Low level output current	I _{OL}	15	mA	General purpose port* ² : per pin
	I _{OLC}	20	mA	High current port* ³ : per pin
Low level total output current	∑I _{OL}	100	mA	Entire pins total
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ V_{CL1}, V_{CL2}, V_{CL3}, V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.*² Specifies the output current of the general purpose I/O port PA to PI, SO, \overline{SC} , PY0 and PY1.*³ The high current operation transistors are the N-ch transistors of the PC and PD ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operation conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Condition

(Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V _{DD}	4.5	5.5	V	Guaranteed range of operation by EXTAL clock
		2.5	5.5	V	Guaranteed range of operation by TEX clock, guaranteed range of data hold during STOP.
LCD bias voltage	V _{CL1} , V _{CL2} , V _{CL3}	V _{SS}	V _{DD}	V	Liquid crystal power supply range* ¹
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input* ²
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin* ³
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input* ²
	V _{ILEX}	-0.3	0.4	V	EXTAL pin* ³
Operating temperature	T _{opr}	-20	+75	°C	

*¹ The optimum value is determined by the characteristics of the liquid crystal display element used.*² The TEX pin when the counter mode is selected by each of INT, RMC, PX0, PX2, PY2, PY3, \overline{RST} pins and mask option.*³ Specified only during external clock input.

Electrical Characteristics

DC characteristics

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit	
High level output voltage	VOH	PA to PI*1 PX0, PX1 PY0, PY1	VDD = 4.5V, IOH = -0.5mA*2	4.0			V	
			VDD = 4.5V, IOH = -1.0mA*2	3.5			V	
			VDD = 4.5V, IOH = -10µA*3	4.0			V	
			VDD = 4.5V, IOH = -200µA*3	2.4			V	
Low level output voltage	VOL	VL (VOL only) RST (VOL only) PC*1, PD*1	VDD = 4.5V, IOL = 1.8mA			0.4	V	
			VDD = 4.5V, IOL = 3.6mA			0.6	V	
			VDD = 4.5V, IOL = 12mA			1.5	V	
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	µA	
	IiLE		VDD = 5.5V, VIL = 0.4V	-0.5		-40	µA	
	IiHT	TEX*4	VDD = 5.5V, VIH = 5.5V	0.1		10	µA	
	IiLT			-0.1		-10	µA	
	IiLR	RST*5	VDD = 5.5V, VIL = 0.4V			-1.5	-400	µA
	IiL	PA*6, PB*6, PE*6, PF*6, PI*6, PX0*6, PX1*6, PX2*8, PY0*7, PY1*7, PY2*8, PY3*8, INT*8, RMC*8, RST*5, TEX*4					±10	µA
High impedance I/O leakage current	IIZ		VDD = 5.5V, VI = 0, 5.5V			±10	µA	
Common output impedance	RCOM	COM0 to COM3	VDD = 5V VLC1 = 3.75V		3	5	kΩ	
Segment output impedance	RSEG	SEG0 to SEG15 SEG16 to SEG31*1	VLC2 = 2.5V VLC3 = 1.25V		5	15	kΩ	
Supply current	IDD1	VDD	Entire output pins open					
			Crystal oscillation (C1 = C2 = 22pF) of VDD = 5.5V, 4.19MHz		7	20	mA	
	IDD2		Crystal oscillation (C1 = C2 = 47pF) of VDD = 3V, 32kHz		50	250	µA	
	IDDSP1		Sleep mode					
			VDD = 5.5V, 4.19MHz oscillation		5	12	mA	
	IDDSP2		VDD = 3V, 32kHz oscillation		40	200	µA	
	IDDS1		Stop mode					
VDD = 3V, 32kHz with T/C			7	40	µA			
IDDS2	VDD = 5.5V, 32kHz without T/C (For mask option select counter, Pin is fixed.)				10	µA		
Input capacity	CIN	Other than VLC1 to VLC3, COM0 to COM3, SEG0 to SEG15, SEG16 to SEG31*1, Vss, VDD pins	Clock 1MHz 0V other than the measured pins		10	20	pF	

- *1 The PC, PD, PG and PH show when the combined pins are selected as the port, and SEG16 to SEG31 show when the combined pins are selected as the segment output.
- *2 It is when the respective pins of PA to PI, PX0 and PX1 select the tri-state output circuit, and PY0 and PY1 are when the inverter output circuit is selected.
- *3 It is when the respective pins of PA to PI, PX0, PX1, PY0 and PY1 select the pull-up resistor.
- *4 The TEX pin specifies the input current when the crystal oscillation is selected by the mask option, and specifies the leakage current when the schmitt input is selected.
- *5 The $\overline{\text{RST}}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.
- *6 The respective pins of PA, PB, PE, PF, PI, PX0 and PX1 specify the input current when the pull-up resistor is selected, and specify the leakage current when the port state during using the tri-state output circuit or standby is selected at high impedance.
- *7 The respective pins of PY0 and PY1 specify the input current when the pull-up resistor is selected, and specify the leakage current when the port state during standby is selected at high impedance.
- *8 The respective pins of PX2, PY2, PY3, INT and RMC only specify the leakage current.

AC characteristics

(1) Clock timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		5	MHz
System clock input pulse width	t _{XL} t _{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	90			ns
System clock input rising and falling times	t _{CR} t _{CF}					200	ns
System clock frequency	f _{CS}	TEX* ² TX	$V_{DD} = 2.5$ to 5.5V Fig. 3		32.768		kHz
Event count clock input pulse width	t _{EL} t _{EH}	$\overline{\text{EC}}$	Fig. 4	t _{sys} * ¹ + 0.05			μs
Event count clock input rising and falling times	t _{ER} t _{EF}	$\overline{\text{EC}}$	Fig. 4			20	ms
Event count input clock input pulse width	t _{TL} t _{TH}	TEX* ³	Fig. 4	10			μs
Event count input clock rising and falling times	t _{TR} t _{TF}	TEX* ³	Fig. 4			20	ms

*1 t_{sys} in the EXTAL input clock is 8/fc.
t_{sys} in the TEX input clock is 4/fcs.

*2 Specified when the crystal oscillation mode is selected by the mask option.

*3 Specified when the counter mode is selected by the mask option.

Note) When adjusting the frequency accurately, there may be cases in which they may differ from Fig. 2.

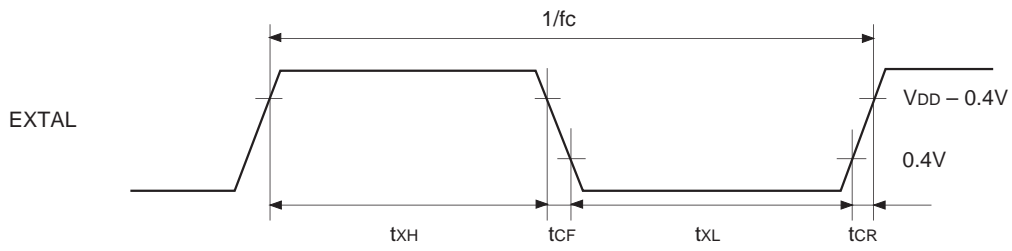


Fig. 1. Clock timing

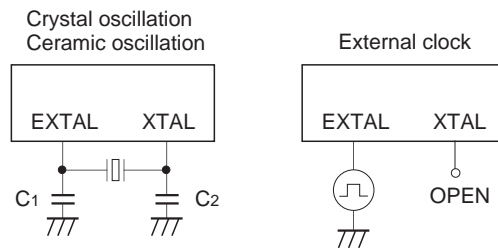


Fig. 2. Clock applying condition

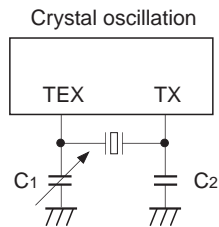


Fig. 3. 32kHz clock applying condition

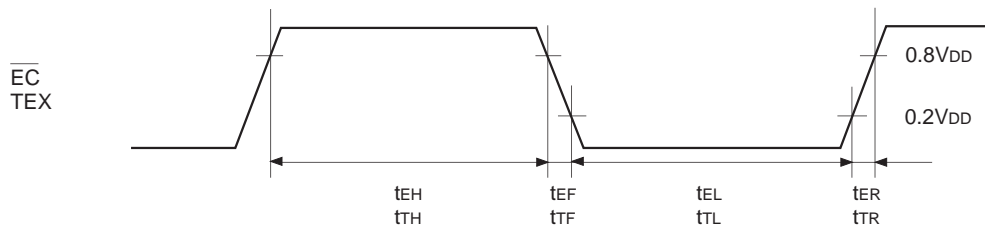


Fig. 4. Event count clock timing

(2) Serial transfer

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Serial transfer clock (\overline{SC}) cycle time	t_{KCY}	\overline{SC}	Input mode	$t_{sys}/4 + 1.42$		μs
			Output mode	$2t_{sys}$		μs
Serial transfer clock (\overline{SC}) high and low level widths	t_{KH} t_{KL}	\overline{SC}	Input mode	$t_{sys}/8 + 0.7$		μs
			Output mode* ¹	$t_{sys} - 0.1$		μs
			Output mode* ²	$t_{sys} - 1.6$		μs
Serial data input setup time (against \overline{SC} \uparrow)	t_{SIK}	SI	\overline{SC} input mode	0.1		μs
			\overline{SC} output mode	0.2		μs
Serial data input hold time (against \overline{SC} \uparrow)	t_{KSI}	SI	\overline{SC} input mode	$t_{sys}/8 + 0.5$		μs
			\overline{SC} output mode	0.1		μs
High data output delay time from \overline{SC} falling* ³	t_{KSO}	SO			$t_{sys}/8 + 0.5$	μs
High data output delay time from \overline{SC} falling* ⁴	t_{KSO}	SO			$t_{sys}/8 + 1.6$	μs
Low data output delay time from \overline{SC} falling	t_{KSO}	SO			$t_{sys}/8 + 0.5$	μs

Notes 1. t_{sys} in the EXTAL input clock is $8/f_c$. (It is impossible to use in TEX input clock.)

2. The load of data output delay is $50pF + 1TTL$.

*¹ It is specified when PX0/ \overline{SC} pin is selected to the tri-state output by the program.

*² It is specified when PX0/ \overline{SC} pin is selected to the pull-up resistance by the program.

As the t_{sys} receives restriction by this item, take notice that it limits the upper limit of the system clock frequency f_c .

*³ This item is specified when PX1/SO pin is selected to the tri-state output by the program.

*⁴ This item is specified when PX1/SO pin is selected to the pull-up resistance by the program.

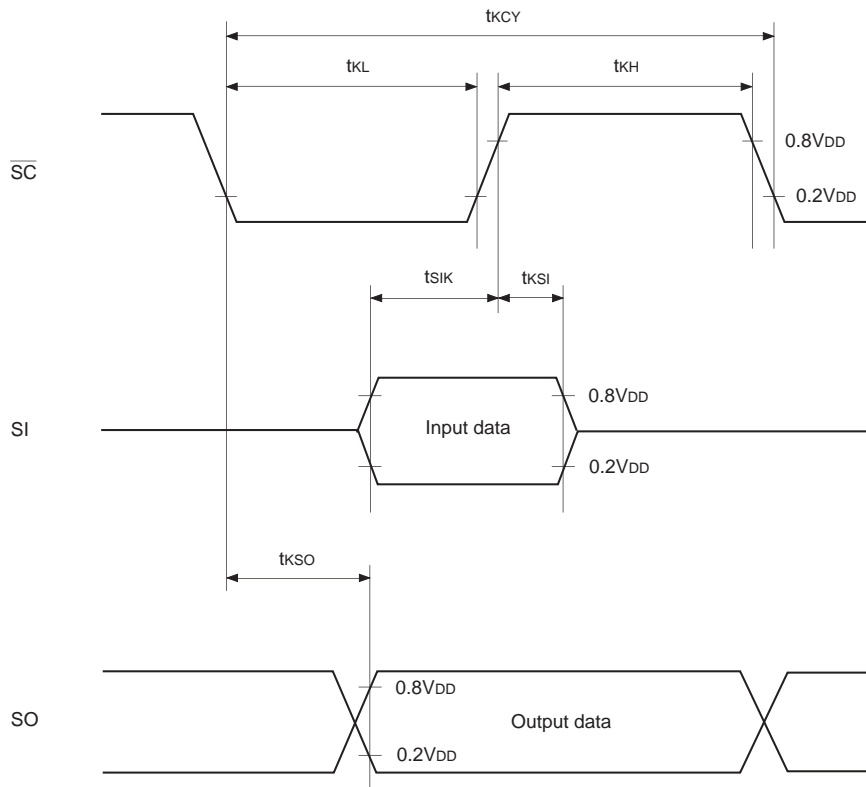


Fig. 5. Serial transfer timing

(3) A/D converter

(Ta = -20 to +75°C, Vss = 0V)

Analog input voltage	Pin	Condition	Digital conversion value
0.0 to 0.33V	AD0 to AD7	V _{DD} = 5V	000
0.82 to 1.29V			001
1.78 to 2.21V			010
2.69 to 3.06V			011
3.56 to 4.06V			100
4.62 to 5.0V			101

Note) The digital conversion value are the values when AB_H address of the RAM file 1 in the program are read.

(4) Power Supply Voltage Detection Reset Function

(Ta = -20 to + 75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply voltage detection reset function of operation voltage range	V _{LPOP}	V _{DD}	Voltage range allowing system operation (32kHz system operation below V _{DD} = 4.5V)	2.5		5.5	V
Power supply voltage drop detection function	V _{POP}	V _{DD}	When V _{REF} pin voltage is 3.3V Flag set when voltage drops System reset when voltage rises	3.8	4.0	4.2	V

The graph in Fig. 6 shows the relationship between the power supply voltage V_{DD} and reference voltage V_{REF} of the power supply voltage detection reset function.

Note) The graph in Fig. 6 serves as guide to the function operation area obtained using average devices.
Individual adjustment is needed when Zener diodes, etc., are connected to the V_{REF} pin.

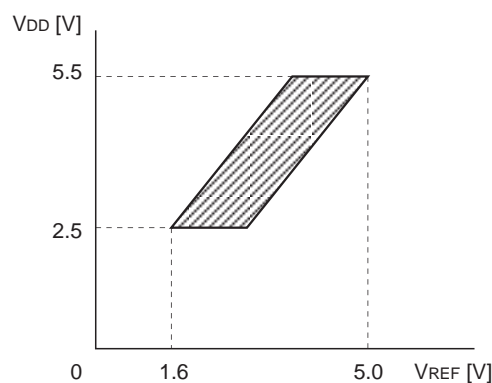


Fig. 6. Power supply voltage detection reset function chart

(5) Others

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{1H} , t_{1L}	INT	During edge detection mode	$t_{sys} + 0.05$		μs
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		$2t_{sys}^{*1}$		μs
Wake-up input high level width	t_{WPH}	WP	Stop mode	500		ns
			Sleep mode	$t_{sys} + 0.05$		μs
Wake-up input low level width	t_{WPL}	PA0 to PA3	Stop mode	500		ns
			Sleep mode	$t_{sys} + 0.05$		μs

Note) t_{sys} in the EXTAL input clock is $8/f_c$.
 t_{sys} in the TEX input clock is $4/f_c$.

*1 For resetting when operating in TEX input clock, hold the low level more than the oscillation stabilizing time of EXTAL input clock.

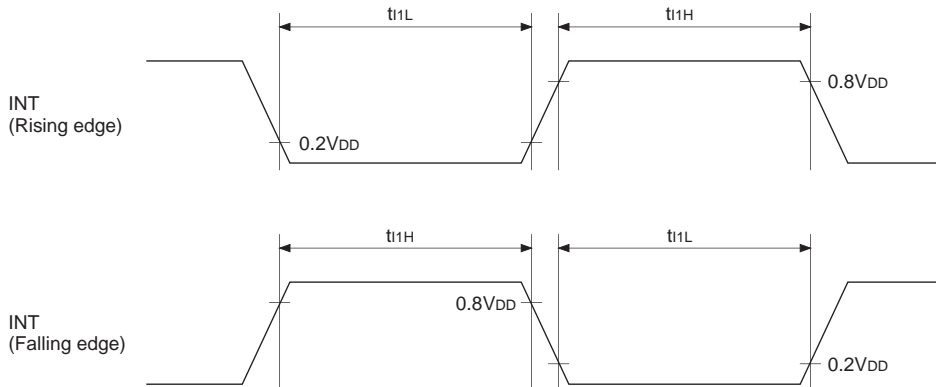


Fig. 7. Interruption input timing

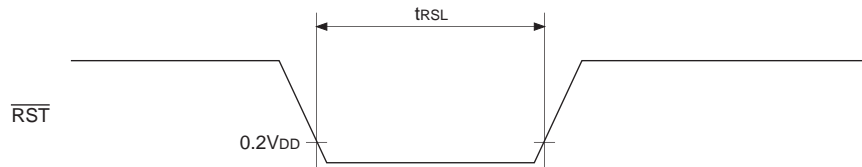


Fig. 8. Reset input timing

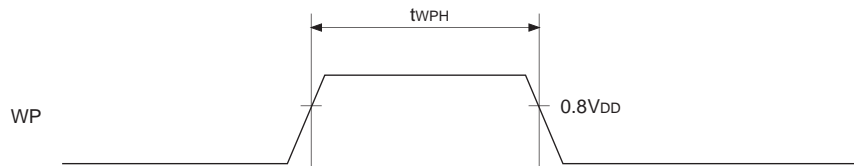


Fig. 9. Wake-up input timing

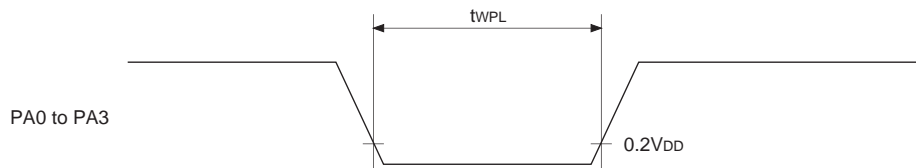


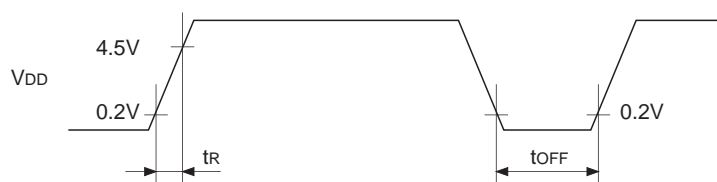
Fig. 10. Wake-up input timing

Power on reset*

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t _R	V _{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t _{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.



The power supply should rise smoothly.

Fig. 11. Power on reset

Notes on Application

See Fig. 11, Additive capacity calculation chart, when using the crystal oscillator and select the appropriate capacity.

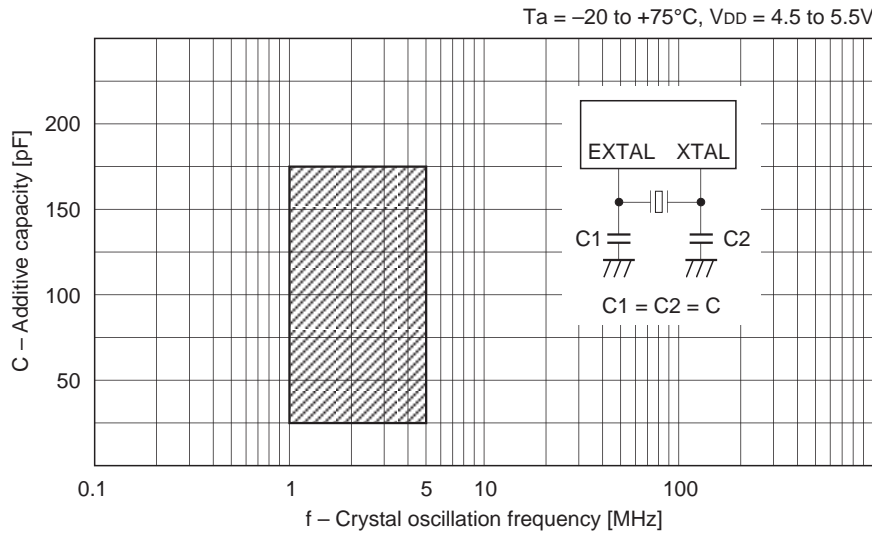


Fig. 12. Crystal oscillation circuit additive capacity calculation chart

Note) The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

Fig. 13 shows an example of a circuit which can accurately adjust the frequency. Used here a trimmer capacitor.

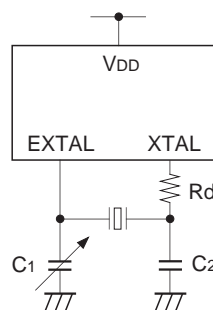


Fig. 13. Frequency adjustment circuit

When using the A/D converter as the key input, it is recommended that the circuit structure shown in Fig. 14 be used.

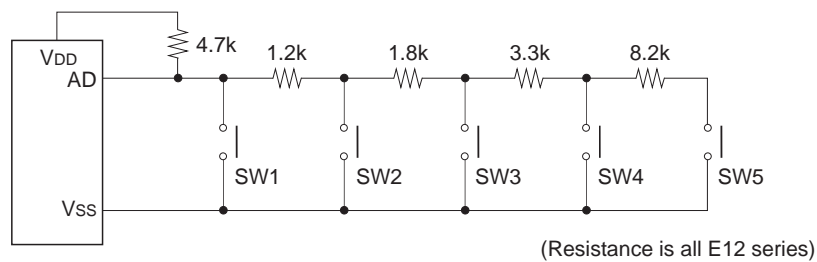
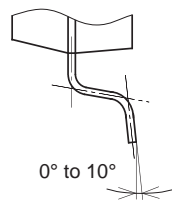
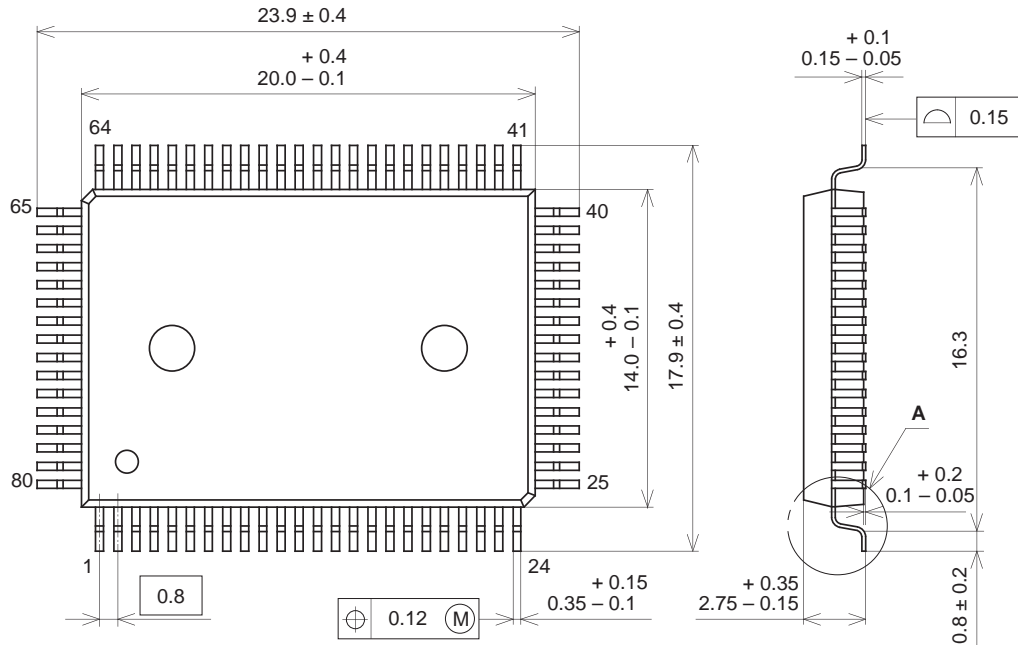


Fig. 14. Recommended example of key circuit by A/D converter

Package Outline Unit: mm

80PIN QFP (PLASTIC)



DETAIL A

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g